**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace, without prejudice, all prior versions and listings of claims in the application.

**LISTING OF CLAIMS:**

1.-14. (Canceled)

15. (Currently Amended) A method for performing an error detection in a cache memory for storing data, the access to the data stored in the cache memory taking place by addresses assigned thereto, comprising:

for the addresses assigned to the stored data, generating and storing in the cache memory at least one first test signature made up of at least one first signature bit; ~~and~~

storing a valid-invalid bit at least in duplicate in the cache memory;

to a group of data and appertaining first test signatures, assigning in each case a first line index in the cache memory;

comparing the first line index to a second line index applied at the cache memory; and

retrieving the first line index from the cache memory by line decoding.

16. (Previously Presented) The method as recited in Claim 15, further comprising:

checking the first test signature for each read access to the cache memory.

17. (Previously Presented) The method as recited in Claim 15, further comprising:

comparing the at least one stored first signature bit of the first test signature to a second signature bit of a second test signature that is formed from an address applied at the cache memory.

18. (Previously Presented) The method as recited in Claim 15, further comprising:

comparing the at least one stored first signature bit of the first test signature to a second signature bit of a second test signature that is transferred together with an address applied at the cache memory.

19. (Canceled)

20. (Previously Presented) The method as recited in Claim 15, wherein the valid-invalid bit is stored m-fold and is checked using an n of m test, m, n being natural numbers and m being > 2 and m>n>m/2.

21. (Previously Presented) The method as recited in Claim 15, wherein the valid-invalid bit is stored k-fold as a bit combination in the form of a 1 of k code, by comparison 1 bit combination of $2^k$ bit combinations being detected as valid, k corresponding to a natural number.

22. (Previously Presented) The method as recited in Claim 15, wherein the data include instructions.

23. (Canceled).

24. (Currently Amended) The method as recited in Claim [[23]] 15, further comprising:
generating an error signal as a function of a comparison result.

25. (Previously Presented) The method as recited in Claim 24, wherein the error signal is treated as a cache miss signal.

26. (Previously Presented) The method as recited in Claim 16, further comprising:
detecting at least one error as a function of a respective comparison result; and
if the at least one error is detected, loading the data into the cache memory in renewed fashion.

27. (Currently Amended) A device for performing an error detection in a cache memory for storing data, the access to the data stored in the cache memory taking place by addresses assigned thereto, comprising:

an arrangement, regarding the addresses assigned to the stored data, for generating and storing in the cache memory at least one first test signature made up of at least one first signature bit, the arrangement further configured to perform: generating and storing in the cache memory a valid-invalid bit at least in duplicate; to a group of data and appertaining first test signatures, assigning in each case a first line index in the cache memory; comparing the first line index to a second line index applied at the cache memory; and retrieving the first line index from the cache memory by line decoding.

28. (Previously Presented) The device as recited in Claim 27, wherein: the device is part of the cache memory.